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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,741	03/22/2004	Wilson E. Taylor	D2A1130-1	9588

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EXAMINER

FLANAGAN, KRISTA M

ART UNIT	PAPER NUMBER
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2817

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/805,741

Applicant(s)

TAYLOR ET AL.

Examiner

Krista M. Flanagan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 March 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10, 12 and 14 is/are rejected.
- 7) ☒ Claim(s) 11 and 13 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 March 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description on page 11 paragraph [0029]: "100". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections – 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2, 3, 8 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Applicants use the term "differential current" but give no clear explanation as to what they regard as a differential current through the claim language or in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 2, 4-12 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Melanson, US Patent No. 6,294,954.

7. Regarding claim 1, Melanson discloses a method of adaptive dead time control for switching circuits with a pulse width modulated control circuit where electrical characteristics (e.g. current and voltage), as disclosed in the reference in column 1, line 61 through column 2, line 16, are measured across the switches by detector block 310 and a control block 320 monitors the timing and sets rise and fall delay of each element thus changing the dead time/overlap to optimize distortion and efficiency as is disclosed in column 2, lines 17-38. As described at column 3, lines 19-26 relative to figure 4, the dead time is incrementally reduced (i.e. adjusted) until overlap is minimized.

8. Regarding claim 2, which inherits all of the limitations of claim 1, in view of the indefinite nature of the term ‘differential current’ as used by the applicant, the Examiner has interpreted the term ‘differential current’ to mean “difference or change in current”.

Accordingly, the prior art reference to Melanson anticipates the Examiner’s interpretation of differential current because Melanson uses a current meter placed in series with the switches to detect the change in the current sensed as the timing is changed from dead time to overlap.

Melanson discloses a method of adaptive dead time control for switching circuits with a pulse

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width modulated control circuit where a current meter placed in series with the switches, as disclosed in the reference in column 1, line 61 through column 2, line 16, measures the current sensed at the switch block as shown in figure 3, blocks 305 and 310.

9. Regarding claim 4, which inherits all of the limitations of claim 1, Melanson discloses a method of adaptive dead time control for switching circuits with a pulse width modulated control circuit where overlap causes current to flow in each transistor and results in 'shoot-through' current, as disclosed in column 1, lines 25-28, which is detected by the measuring block 310.

10. Regarding claims 5 and 6, which inherit all of the limitations of claims 4 and 1 respectively, Melanson discloses a method of adaptive dead time control for switching circuits with a pulse width modulated control circuit where the current measured by block 310 changes at the transition between dead time and overlap causing 'distortion' as described in column 1, lines 62-65.

11. Regarding claim 7, Melanson discloses an adaptive dead time control for switching circuits with a pulse width modulated control circuit shown in figure 3, block 101; drivers shown in figure 3, blocks 302 and 303; switch block shown in figure 3, block 305; and control circuitry shown in figure 3, blocks 310, 320 and 322; wherein the drivers are coupled between the PWM control and the switch block, wherein the drivers are configured to receive high-side and low-side PWM signals from the PWM control and to drive the high side and low side PWM control signals to the switch block; wherein the control circuitry is coupled between the switch block and the PWM control, wherein the control circuitry is configured to provide feedback associated with dead time /overlap (i.e. resulting in 'shoot-through' current) in the switch block to the PWM control shown by blocks 310 and 320 in figure 3; and wherein the PWM control is configured to

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adjust the relative timing of the high-side and low-side PWM signals in response to the feedback through control block 320 and control signal 322 to optimize the dead time /overlap in the switch block as disclosed at column 3, lines 8-18.

12. Regarding claim 8, which inherits all of the limitations of claim 7, in view of the indefinite nature of the term 'differential current' as used by the applicant, the Examiner has interpreted the term 'differential current' to mean "difference or change in current".

Accordingly, the prior art reference to Melanson anticipates the Examiner's interpretation of differential current because Melanson uses a current meter placed in series with the switches to detect the change in the current sensed as the timing is changed from dead time to overlap.

Melanson discloses a system of adaptive dead time control for switching circuits with a pulse width modulated control circuit where a current meter placed in series with the switches, as disclosed in the reference in column 1, line 61 through column 2, line 16, measures the current sensed at the switch block as shown in figure 3, blocks 305 and 310.

13. Regarding claim 10, which inherits all of the limitations of claim 7, Melanson discloses a system of adaptive dead time control for switching circuits with a pulse width modulated control circuit where overlap causes current to flow in each transistor and results in 'shoot-through' current, as disclosed in column 1, lines 25-28, which is detected by the measuring circuit 310.

14. Regarding claims 12 and 14, which inherit all of the limitations of claims 10 and 7 respectively, Melanson discloses a system of adaptive dead time control for switching circuits with a pulse width modulated control circuit where the current measured by block 310 changes at the transition between dead time and overlap causing 'distortion' as described in column 1, lines 62-65.

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Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

16. Claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Melanson, US Patent No. 6,294,954 in view of Aiello, US Patent No. 4,554,512.

17. Regarding the claims, which inherit the limitations of claim 2 and 8 respectively, Melanson discloses a method and system of adaptive dead time control for switching circuits with a pulse width modulated control circuit where the PWM control is configured to adjust the relative timing of the high-side and low-side PWM signals in response to the feedback to optimize the dead time /overlap in the switch block as disclosed at column 3, lines 8-18. Melanson fails to disclose the PWM control configured to provide each high side and low side signal at a 50% duty cycle. However, Aiello discloses a switching amplifier wherein a PWM modulator is configured to provide each of the high-side and the low-side signals of the transistors at a 50% duty cycle shown in figures 5a and 5b (where the high side is on half the time and the low side is on half the time), and to adjust the relative timing between the high-side signal and the low-side signal to minimize the current at the load as disclosed in column 5, lines 34-59 and column 6, lines 12-17. One would be motivated to do this because a 50% duty cycle would optimize conditions to avoid overlap. Therefore, at the time the invention was made, it would have been obvious to one of ordinary skill in the art to provide the low and high side signals at a 50% duty cycle.

Allowable Subject Matter

18. Claims 11 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. The following is a statement of reasons for the indication of allowable subject matter:

20. Regarding claim 11, which inherits all of the limitations of claim 10, prior art discloses a switching amplifier but fails to disclose a switching amplifier wherein the feedback circuitry includes a resistor coupled in series with a pair of output stage transistors, and a comparator configured to measure a voltage drop across the resistor and compare the measured voltage drop to a threshold level.

21. Regarding claim 13, which inherits all of the limitations of claim 12, prior art discloses a switching amplifier wherein the feedback circuitry includes dead time or "distortion" circuitry but fails to disclose a switching amplifier wherein the dead time circuitry is configured to measure one or more harmonics of the output signal produced by the output stage.

Conclusion

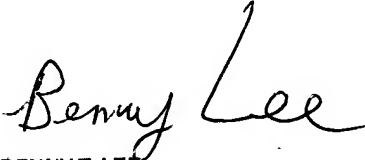
22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Krista M. Flanagan whose telephone number is (571) 272-2203. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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20050721


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PRIMARY EXAMINER
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